1. An asymmetric digital subscriber loop modem comprising:

an integrated circuit;

an analog-to-digital converter contained in said integrated circuit, said converter producing data at a relatively higher data rate;

a device contained in said circuit and coupled to said analog-to-digital converter, said device reducing the higher data rate data from the analog-to-digital converter to a lower data rate; and

a multiplexer that multiplexes said lower data rate data and control information and transmits said data and control information externally of said integrated circuit.

2. The modem of claim 1 including a second integrated circuit, said second integrated circuit including a de-multiplexer that de-multiplexes said lower data rate data and said control information.

3. The modem of claim 1 wherein said device includes a decimation filter.

4. The method of claim 3 wherein said integrated circuit includes a analog filter coupled to said analog-to-

digital converter in turn coupled to said decimation filter in turn coupled to said multiplexer.

5. The modem of claim 1 wherein said integrated circuit further includes a demultiplexer coupled to a device that increases the data rate of data received by said demultiplexer, said device that increases the data rate being coupled to a digital-to-analog converter.

6. The modem of claim 5 wherein said device for increasing the data rate includes an interpolation filter.

7. The modem of claim 1 wherein said integrated circuit includes both a receiver section and a transmitter section.

8. The modem of claim 1 including a second integrated circuit having a receiver section coupled to receive said lower data rate data and control information from said integrated circuit.

9. The modem of claim 8 wherein said second integrated circuit implements discrete multi-tone modulation.

10. The modem of claim 9 wherein said second integrated circuit provides digital signal processing.

11. The modem of claim 9 wherein said second integrated circuit includes a fast Fourier transformer and a line decoder.

12. The modem of claim 1 including a second integrated circuit, said second integrated circuit including a line encoder which produces data at a relatively higher data rate and a device coupled to said line encoder that produces data at a relatively lower data rate, said device being coupled to a serializer which transmits said data to said integrated circuit.

13. The modem of claim 12 wherein said device is an inverse fast Fourier transformer.

14. A method comprising:

receiving analog data on a first integrated circuit device;

converting said analog data to digital format;

decreasing the data rate of said data;

serializing said data; and

transmitting said data to a second integrated circuit device.

15. The method of claim 14 wherein reducing the data rate of said digital data includes decimating said digital data.

16. The method of claim 15 wherein serializing said data includes multiplexing said data with control information.

17. The method of claim 16 further including receiving said data on said second integrated circuit and de-serializing said data.

18. The method of claim 17 including increasing the data rate of said data on said second integrated circuit.

19. The method of claim 18 wherein increasing said data rate includes fast fourier transforming said data.

20. The method of claim 14 further including receiving digital data for transmission by said first chip and increasing the data rate of said data.

21. The method of claim 20 wherein increasing said data rate includes interpolating said data.

22. The method of claim 21 including converting said interpolated data to an analog format signal.

23. An asymmetric digital subscriber loop modem comprising:

a first integrated circuit including an analog-to-digital converter, a device to reduce the data rate from the analog-to-digital converter to a lower data rate, and a serializer; and

a second integrated circuit, said serializer transmitting said lower data rate data from said first integrated circuit to said second integrated circuit, said second integrated circuit including a de-serializer that receives said lower data rate data from said first integrated circuit and transmits said data to a device for demodulating said data.

24. The modem of claim 23 wherein said second integrated circuit includes a modulating circuit which decreases the data rate of digital data and a serializer which transmits said decreased data rate data to said first integrated circuit, said first integrated circuit including a de-serializer that receives said modulated data, said de-serializer coupled to a device that increases the data rate of said data, said device coupled to a digital-to-analog converter.

25. The modem of claim 23 wherein said device on said first integrated circuit for decreasing the data rate of said data is a decimation filter.

26. The modem of claim 24 wherein said device that increases the data rate on said first integrated circuit is an interpolation filter.

27. The modem of claim 24 wherein said modulating circuit includes an inverse fast Fourier transformer.

28. The modem of claim 23 wherein said modem is a splitterless remote modem.

29. The modem of claim 23 wherein said serializer multiplexes lower data rate data and control information.

30. The modem of claim 23 wherein lower data rate data is transmitted in two directions between said first and second integrated circuits.